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Memory Optmization In Map Decoding Algorithm Using Trace Forward Technique In Turbo Decoder By Using Of VLSI Implementation

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Abstract

Iterative decoding of convolutional turbo code (CTC) has a large memory power consumption. To reduce the power consumption of the state metrics cache (SMC), low-power memory-reduced traceforward maximum a posteriori algorithm (MAP) decoding is proposed. Instead of storing all state metrics, the trace forward MAP decoding reduces the size of the SMC by accessing difference metrics. The proposed trace forward computation requires no complicated forward checker, path selection, and reversion flag cache. For double-binary (DB) MAP decoding, radix-2X2 and radix-4 trace forward structures are introduced to provide a tradeoff between power consumption and operating frequency. These two traceforward structures achieve an around 20% power reduction of the SMC, and around 7% power reduction of the DB MAP decoders. In addition, a high-throughput 12-mode WiMAX CTC decoder applying the proposed radix-2 2 trace forward structure is implemented by using a 0.13- m CMOS process in a core area of 7.16 mm. Based on post layout simulation results, the proposed decoder achieves a maximum throughput rate of 115.4 Mbps and an energy efficiency of 0.43 nJ/bit per iteration.

Keywords: Low-power design, maximum a posteriori (MAP algorithm, turbo decoder.

Introduction

SINGLE-BINARY (SB) convolutional turbo code (CTC), proposed in 1993, has been proven to provide a high coding gain near the Shannon capacity limit. The SB-CTC has been adopted in the forward-error-control (FEC) scheme for wideband code-division multiple access (WCDMA) and cdma2000. In 1999, the no binary CTC was introduced, which a superior coding performance has compared with the SB CTC. In recent years, double-binary (DB) CTC has been adopted in the FEC coding of advanced wireless communication standards, such as digital video broadcasting-return channel over satellite and terrestrial (DVB-RCS and DVB-RCT), and worldwide interoperability for microwave access (WiMAX). Powerful soft-input soft-output (SISO)

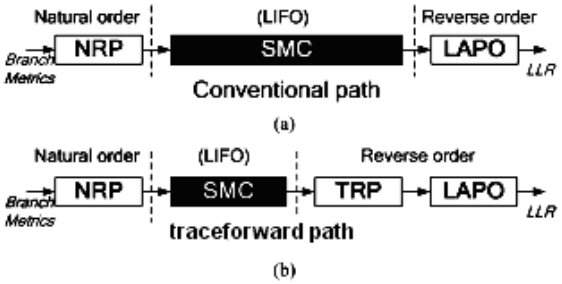

Fig. 1. Decoding path of the state metrics access: the (a) conventional path and (b) trace forward path

Algorithms for CTC decoding are the maximum a posteriori algorithm (MAP), and its derivatives, such as the log-MAP (L-MAP), Max-log-MAP (ML-MAP), combinations of the L-MAP and ML-MAP, and enhanced Max-log-MAP (EML-MAP). In this paper, we use the term MAP for an abbreviation of L-MAP and (E) ML-MAP. The memory organization of MAP decoding is an important issue in facilitating the hardware implementation of CTC decoders. In particular, the power reduction of state metrics cache (SMC) is critical for MAP decoders. With regard to SB CTC decoding, some researches have been proposed to reduce the power consumption of the SMC. The reverse computations significantly reduce SMC power consumption with forward checkers and forward flag caches. However, the forward checker and forward flag cache prolong the critical path or decoding cycles. In addition, the computational complexities of the forward computations are increased dramatically when the forward computations are extended from the SB to the DB MAP.

In this is paper, the trace forward MAP decoding is proposed to trace the state metrics back by accessing the difference metrics. Fig. 1 illustrates the decoding paths of the conventional computation and proposed traceforward computation. In the conventional path, the state metrics computed by the natural recursion processor (NRP) in the natural order are

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stored in the SMC. Then, the state metrics are read out to compute the a posteriori log-likelihood ratio (LLR) by the log-a posteriori (LAPO) module in the forward reverse order.

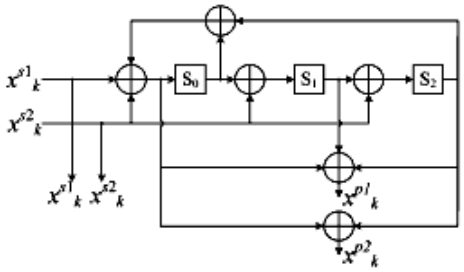

Fig. 2. DB RSC encoder of WiMAX CTC scheme.

In the trace forward path, the difference metrics computed by the NRP are stored in the SMC. Then, the state metrics are traced forward with the stored difference metrics by the trace forward recursion processor (TRP) in the reverse order. The power consumption of the SMC can be reduced by accessing the difference metrics because the number of stored metrics is lower. The computational power of TRP is small, and the overall power consumption of the trace forward path is reduced. For the trace forward DB MAP decoding, two trace forward structures are demonstrated. The radix-2X2 trace forward structure has low hardware costs, and the radix-4 trace forward structure has short path delays. Experimental results show that these two trace forward structures achieve an around 20% power reduction of the SMC, and around 7% power reduction of the DB MAP decoder.

In addition, an application of the proposed trace forward DB MAP decoding for the DB CTC is to deploy the radix-2X2 trace forward structures to a high-throughput WiMAX CTC decoder. We emphasize the 12 general transmissions of the WiMAX CTC scheme without the optional hybrid automatic repeat request (HARQ) transmissions. The 12-mode CTC decoder was implemented by using a TSMC 0.13 m CMOS process. The prototyping chip in a core area of 7.16 mm achieves 115.4 Mbps, with an energy efficiency of 0.43 nJ/bit per iteration.

traceforward structures. The prototyping chip of the 12-mode WiMAX CTC decoder is described in Section VII. Finally, Section VIII concludes this paper.

Reviews of DB Map Decoding

A CTC encoder is composed of a CTC interleaver and two parallel or serial concatenated recursive systematic convolution (RSC) encoders. Fig. 2 shows the DB RSC encoder of a WiMAX CTC scheme. The constraint length v of this DB RSC encoder is 4.

The transmitted code words are denoted by $x_k^{s1}, x_k^{s2}, x_k^{p1}$ and x_k^{p2}.

Powerful SISO algorithms for DB CTC decoding are the DB MAP. First, the arithmetic operations of the DBEML-MAP are described as follows:

$$\gamma_k^{(z)}(S_{k-1}, S_k) = \Lambda_{\mathrm{apr},k}^{(z)}(u_k = z) + 2y_k^{s1}x_k^{s1} + 2y_k^{s2}x_k^{s2} + 2\sum_{i=1}^{m} y_k^{pi}x_k^{pi} \quad (1a)$$

$$\alpha_k(S_k) = \underset{S_{k-1}}{\mathrm{MAX}}\left(\gamma_k^{(z)}(S_{k-1}, S_k) + \alpha_{k-1}(S_{k-1})\right) \quad (1b)$$

$$\beta_k(S_k) = \underset{S_{k+1}}{\mathrm{MAX}}\left(\gamma_{k+1}^{(z)}(S_k, S_{k+1}) + \beta_{k+1}(S_{k+1})\right), \quad (1c)$$

$$\Lambda_{\mathrm{apo},k}^{(z)}(u_k) = \underset{S_{k-1},S_k,u_k=z}{\mathrm{MAX}}\left(\alpha_{k-1}(S_{k-1}) + \gamma_k^{(z)}(S_{k-1}, S_k) + \beta_k(S_k)\right) - \underset{S_{k-1},S_k,u_k=00}{\mathrm{MAX}}\left(\alpha_{k-1}(S_{k-1}) + \gamma_k^{(00)}(S_{k-1}, S_k) + \beta_k(S_k)\right) \quad (1d)$$

where

$\gamma_k^{(z)}$	branch metrics;
α_k	forward recursion state metrics;
β_k	backward recursion state metrics;
$\Lambda_{\mathrm{apr},k}^{(z)}$	*a priori* LLR;
$\Lambda_{\mathrm{apo},k}^{(z)}$	*a posteriori* LLR;
$\Lambda_{\mathrm{in},k}^{(z)}$	intrinsic values;
$x_k^{s1}, x_k^{s2}, x_k^{pi}$	transmitted codewords $\in \{-1, +1\}$ for BPSK;
$y_k^{s1}, y_k^{s2}, y_k^{pi}$	soft received codewords;
m	number of parity bit;
z	$\in \{00, 01, 10, 11\}$;
S_k	state index;
δ	scaling factor $(0 < \delta < 1)$.

Decisions $u_k = z$ are based on

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$$z = \arg_z \left(\mathrm{MAX} \left(\Lambda^{(00)}_{\mathrm{apo},k}(u_k), \Lambda^{(01)}_{\mathrm{apo},k}(u_k), \Lambda^{(10)}_{\mathrm{apo},k}(u_k), \Lambda^{(11)}_{\mathrm{apo},k}(u_k) \right) \right)$$

(2) Note that the values of , and $\Lambda^{(00)}_{\mathrm{in},k}$ are always equal to zero. The differences between the DB L-MAP and DB (E)ML-MAP are that a priori LLR multiplies the channel value, and MAX operations are replaced by in the DB L-MAP. The is defined as

$$\mathrm{MAX}^*(x,y) = \ln(e^x + e^y) = \mathrm{MAX}(x,y) + \ln(1+e^{-|x-y|}).$$

A lookup table (LUT) can implement the corrective ln(1+e-x-y). term. The difference between the DB EML-MAP and DB ML-MAP is that the extrinsic values in the DB ML-MAP do not multiply a scaling factor. Despite the SB and DB MAP decoding, the L-MAP has the significant coding gain and the EML-MAP achieves better coding gain than the ML-MAP. Without specifying which algorithm is used, we use the term MAP for an abbreviation of the L-MAP and (E)ML-MAP in the following sections. The details of SB MAP algorithms can be referred to in [10] for the SB CTC.

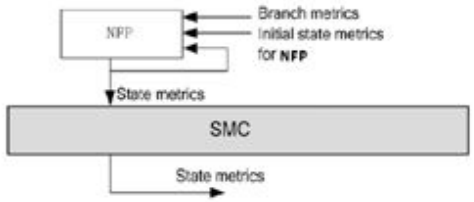
Power Reductions of State Metrics Cache

Before we introduce the proposed memory-reduced trace forward MAP decoding, the background information of SMC power reduction for the MAP decoding is demonstrated in this section.

A. Conventional (Windowing) Decoding Procedure

Despite the SB or DB MAP decoding,2v-1 forward(1b) recursion states metrics are computed in chronologically forward order, where *v* is the constraint length of a RSC encoder. Both forward recursion state metrics are required for the computation of a posteriori LLR(1d). Thus, a large SMC stores the forward recursion state metrics to compute the a posteriori LLR until the forward recursion state metrics are generated. The conventional decoding procedure employing the windowing technique was proposed to reduce the depth of SMC from a block size(N) to a window size(L), where L is 4*v* . (The well-known sliding window (SW) and parallel window (PW) MAP architectures can be referred respectively.) Fig. 3 shows the conventional decoding procedure. In the natural order, the NRP, composed of add-compare-select units (ACSUs), is used to recursively compute the forward recursion state metrics in cycles. The obtained state metrics in each cycle are immediately stored into the SMC and recursively fed back to the NRP to calculate the next state metrics. To compute the a posteriori LLR, the state metrics are read out from the SMC. The SMC of the conventional decoding procedure still accounts for more than 50% of the entire power consumption.

Fig. 3. Conventional decoding procedure



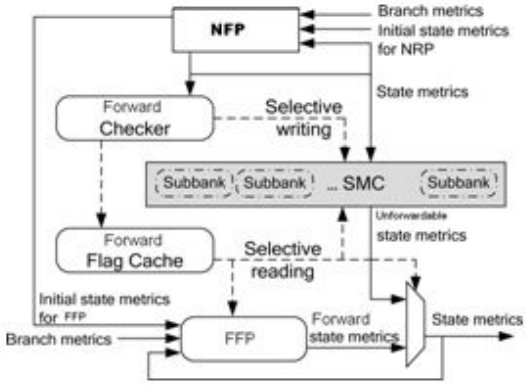


Fig. 4. Reverse decoding procedure

B. Decoding Forward Procedure

To further reduce the access power of SMC, the reverse computations modified the conventional decoding procedure for the radix-2 SBMAPdecoding. The decoding procedure of the reverse computations is illustrated in Fig. 4. Compared with the conventional decoding procedure shown in Fig. 3, the reverse decoding procedure adds a reversion checker, a reversion flag cache, and a reverse recursion processor (RRP). The reversion checker decides whether the state metrics computed by the NRP are reversible or not. If a state metric is not reversible, this state metric is stored in one sub bank of the SMC. Meanwhile, the reversion flag cache stores the path information of this state metric. To compute the a posteriori LLR, the irreversible state metric is read out from the SMC according to the path information stored in the reversion flag cache. Otherwise, the reversible state metric is computed by the FRP, composed of reverse units. The recovered state metrics are recursively fed back to the FRP to calculate the next reversible state metrics.

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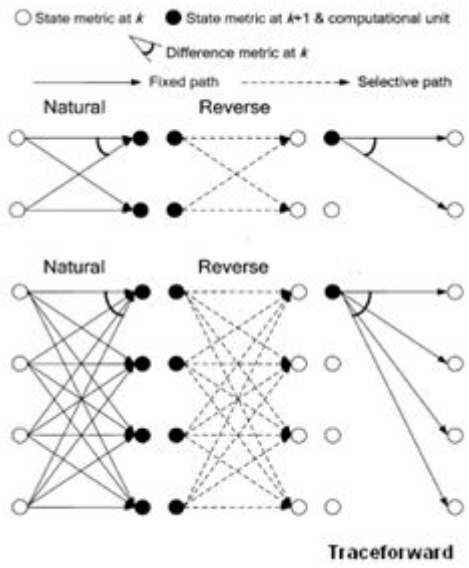

Fig. 5. Natural, reverse, and trace forward recursions in the (a)–(c) radix-2 butterfly structures and (d)–(f) radix-4 butterfly structures. The symbol index is denoted by □. For the conversional decoding procedure, the computational units in (a) are the ACSUs. For the reverse decoding procedure, the computational units in (a) and (d) are the ACSUs and forward checkers, and the computational units in (b) and (e) are the reverse units. For the trace forward decoding procedure, the computational units in (a) and (d) are ACSUs only, and the computational units in (c) and (f) are the TBUs.

The reverse computations reduce the power consumption of the radix-2 SB MAP decoder because the sub banks of SMC are dynamically accessed, and the computational power of the reversion checker and RRP is small. The reverse computations for the radix-2 SB L-MAP decoding achieve an around 30% power reduction with over 20% logic overhead. However, the forward checker and forward flag cache prolong the critical path or decoding cycles. In addition, dividing the SMC into sub banks increases the silicon area of the SMC and consumes more overall power of the SMC if all sub banks are accessed. For the radix-2 SB MAP decoding, a-state trellis structure can be decomposed into radix-2 butterfly structuresFig. 5(a) and (b) illustrates an example of the SB reverse computation in a radix-2 butterfly structure. In Fig. 5(a), the reversion checker checks all fixed paths and determines the reversible paths. In Fig. 5(b), the dashed lines denote the reversible (selective) paths determined by the reversion flag cache. One radix-2 butterfly structure has four paths and four cases to be checked.

Proposed Memory-Reduced Traceforward Map Decoding

Here, the trace forward MAP decoding is proposed to reduce the power consumption of the SMC. The trace forward MAP decoding has five major stages/phases, given here.

1) The branch metrics are computed with the received code words and the a priori LLR in the natural order.

2) The forward state metrics are recursively computed by the NRP with the branch metrics in the natural order, and the difference metrics are stored into the SMC. Note that the difference metric is the difference between two state metrics and has the same bit-length of the state metric.

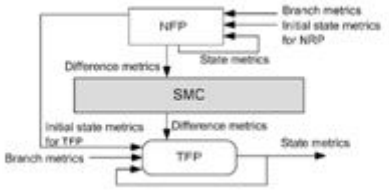

Fig. 6. Trace forward decoding procedure

3) The forward state metrics are recursively traced forward by the TRP with the stored difference metrics in the reverse order. Concurrently, the forward state metrics are recursively computed with the branch metrics.

4) The a posteriori LLR is computed with regenerated forward state metrics, the forward state metrics, and branch metrics by the LAPO in the forward order.

5) The extrinsic values and hard bits are computed in the reverse order with the a posteriori LLR. In contrast to the conventional MAP decoding, the trace forward MAP decoding reduces the number of stored metrics by accessing the difference metrics. Hence, the SMC power consumption is reduced. In addition, the computational power overhead of tracing the state metrics back is much smaller than the SMC power consumption. Thus, the overall power consumption of the MAP decoding is reduced. The work in has introduced that not absolute values but differences between the state metrics are important for the a posteriori LLR. In the proposed trace forward computation, the differences between state metrics are kept by storing the difference metrics. Hence, the trace forward MAP decoding performs without losing correction ability. In addition, the proposed trace forward computation works in the L-MAP and (E)ML-MAP. Fig. 6 shows the proposed trace forward decoding procedure, which is a modification of the conventional decoding procedure shown in Fig. 3. Compared with the conventional decoding procedure, only an additional TRP is added. Fig. 5(a) and (c) illustrates an example of the radix-2 SB trace forward computation in a radix-2 butterfly structure. In Fig. 5(a), only one difference

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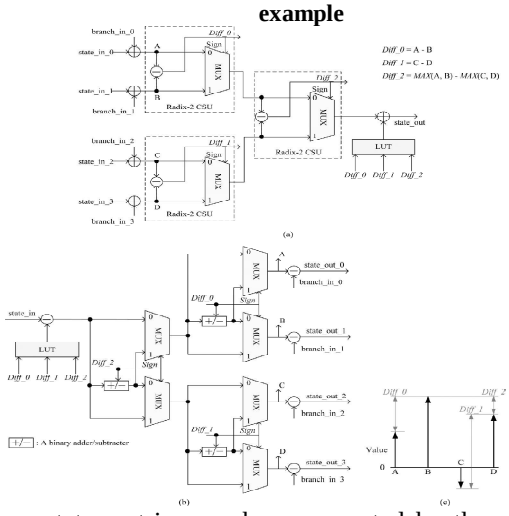
metric (black arc) computed by a radix-2 ACSU is stored in the SMC. In Fig. 5(c), the two state metrics (white nodes) are traced back in the trace forward recursion by one trace forward unit (TBU) with the stored difference metric (black arc). The recovered two state metrics are recursively fed back to the TRP to calculate the next two state metrics. The stored metrics are reduced from two state metrics to one difference metric. The bit-lengths of the state metric and difference metric are the same. Thus, the radix-2 trace forward SB MAP decoding requires half the SMC size of the conventional decoding procedure. Compared with the reverse computations shown in Figs. 4 and 5(b), the trace forward computation has fixed paths and requires no complicated checker and path selection. The design details of the radix-2 trace forward SB MAP decoding, including the radix-2 ACSU, radix-2 TBU, and overall architecture of the WCDMA CTC decoder, can be referred to in. Based on the experimental results using a 0.18-m CMOS process, the radix-2 SB trace forward MAP decoding achieves a 21.4% power reduction of the SW L-MAP decoder with a 3.2% logic overhead.

Radix-2X2 Traceforward Pair

The radix-2x2 ACSU widely used to constitute the NRP. Fig. 8(a) shows an example of the radix-2x2 ACSU. The radix-2x2 ACSU consists of four front adders, three radix-2 compare-select units (CSUs), and an LUT. In the proposed trace forward computation, three difference metrics (Diff 0, Diff 1, and Diff 2) generated by three radix-2 CSUs are stored in the SMC. Fig. 8(b) shows the corresponding TBU of the radix-2x2 ACSU. Fig. 8(c) illustrates a computational example of the radix-2x2 ACSU and TBU. The radix-2x2 ACSU obtains the maximal state metric B based on Diff 0, Diff 1, and Diff 2. Subsequently, the radix-2x2 TBU
Regenerates A, B, C, and D based on Diff 0, Diff 1, and Diff 2, since B can be initially achieved. Hence,

Fig. 8. Radix-2x2 trace forward pair: (a) the ACSU, (b) the TBU, and (c) a computational example



the four state metrics can be recomputed by the radix-2x2 TBU with the difference metrics stored in the SMC. In the radix-2x2 TBU, the sign bit of the difference metric decides the paths of the two multiplexers and the operation of the binary adder/subtracted. Taking the trellis diagram shown in Fig. 7(b), for instance, six difference metrics are stored in the SMC because two current states and two TBUs can trace eight next states back. The storage of the SMC is reduced from eight state metrics to six difference metrics at each stage. Note that the values A, B, C, and D in the output end of the radix-2x2 TBU can be the input values of the LAPO to compute . This approach reduces eight adders (or in (1d)) in the LAPO.

Experimental Features

Here, accurate silicon area and power evaluations are obtained by using Verilog HDL codes synthesized with the standard cell library of TSMC 0.13-m CMOS process. Taking and , for instance, eight radix-2x2 ACSUs generate eight state metrics at each time stage. Hence, the SMC of the conventional structures has 80 bit-lengths. However, the trace forward structure composed of eight radix-2x2 ACSUs and two radix-2x2 TBUs reduces the SMC bit-lengths from 80 to 60.. The size of information bits is a double of a block size because of the DB CTC. The bit-length of a state metric or a difference metric is 10.The radix-2x2 ACSU has the longest path delay, because the values of the latter radix-2 CSU in the radix-2x2 ACSU are not correct until the sign (most significant) bits of the two former radix-2 CSU are stable. The radix-2x2 TFU does not suffer from this problem because the sign bits of the difference metrics are initially known.

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TABLE I: Computational Unit For 2x2 Radix Structures

Structure	Unit	Path Delay (ns)	Area (μm^2)	Power (mW)
Radix – 2x2 Conventional	NFP (4ACSUs)	9.28	18535.6	0.61

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